Modeling the Drain Current of the Dual-Gate GaAs MESFET

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***Abstract* — A new empirical model of the dual-gate GaAs MESFET (DGFET) drain current is presented. The model uses a modified expression of the well-established hyperbolic tangent-function to accurately fit the DC and the RF I/V characteristics of the DGFET. The frequency dispersion of the DGFET transconductances and output conductance is taken into account in the new model. The new model is tested on many devices of different topologies. Very good agreement between the measured and the calculated I/V characteristics over a wide range of bias conditions is achieved.**

I. INTRODUCTION

While several models of the SGFET drain current have been reported [1-3], much less has been published to model the DGFET drain current [4-6]. Except for Jenner's model [6], all the published models deal with the DGFET as a cascode connection of two SGFETs, FET_1 and FET_2, where each FET part has a current generator that represents the drain current flowing in this particular part. These models [4,5] did not fit the measured data well.

On the other hand, Jenner [6] represented the drain current by a current generator and used a three-dimensional power series expression to model the drain current of the DGFET. To obtain good accuracy, a large number of model parameters are needed. This number can be as large as 165.

None of the above models [4-6] took into consideration the frequency dispersion of the DGFET transconductances and output conductance.

Recently, the authors successfully developed a large-signal model of the DGFET (to be submitted for publication). The developed large-signal model for a grounded-source DGFET is shown in Fig. 1. The charge sources Q_{g1}, Q_{g2}, and Q_d model the displacement current of $gate_1$, $gate_2$, and the drain terminals respectively. The current source I_d models the drain current. The current source I_{g1f} models $gate_1$ forward current while the current sources I_{g2fs} and I_{g2fd} model $gate_2$ forward current flowing to the source and to the drain respectively. The current sources I_{g1bd} and I_{g2bd} model the breakdown current of $gate_1$ and $gate_2$ respectively.

In this work the authors introduce a new empirical model of the DGFET drain current using a nonlinear expression of the current generator I_d as a function of the three applied intrinsic voltages, $gate_1$-source voltage (V_{g1s}), $gate_2$-source voltage (V_{g2s}), and drain-source voltage (V_{ds}).

This model has 49 parameters, which is a much smaller number than the 165 parameters in Jenner's [6] model. The developed equations successfully model the DC drain current (I_{dc}^{DC}) as well as the RF drain current (I_{dc}^{RF}). The bias dependent frequency dispersion is taken into consideration in this model by expanding the method suggested by Root, Fan and Meyer [7] for the SGFET to be used to model the drain current of the DGFET. The total DGFET drain current is then given by:

$$I_d = h(f) I_d^{DC} + [1 - h(f)] I_d^{RF} \tag{1}$$

The first term of (1) models the DC drain current while the second term models the RF drain current. The function h(f) is used to make a smooth transition from the DC current function to the RF current function. However, since the interest is in modeling the DGFET characteristics at DC or at RF (f > 45 MHz), h(f) need not be smooth and is approximated here as a step function [8]:

$$h(f) = \begin{cases} 1 & f = 0 \\ 0 & f > 0 \end{cases} \tag{2}$$

II. THE DC DRAIN CURRENT GENERATOR

The following empirical model is developed by the authors to accurately model the DGFET DC drain current

$$I_d^{DC}(V_{g1s}, V_{g2s}, V_{ds}) = f_1(V_{g1s}, V_{ds}) f_2(V_{g2s}, V_{ds}) f_3(V_{g1s}, V_{g2s}, V_{ds}) \tag{3}$$

where $f_1(V_{g1s},V_{ds})$, $f_2(V_{g2s},V_{ds})$, and $f_3(V_{g1s},V_{g2s},V_{ds})$ are given by:

$$f_1(V_{g1s},V_{ds}) = \{(a_0+a_1V_{ds})+(a_2+a_3V_{ds})V_{g1s} + (a_4+a_5V_{ds})V_{g1s}^2+(a_6+a_7V_{ds})V_{g1s}^3 + (a_8+a_9V_{ds})V_{g1s}^4+(a_{10}+a_{11}V_{ds})V_{g1s}^5 + (a_{12}+a_{13}V_{ds})V_{g1s}^6\}\{a_{14}+a_{15}V_{ds}+a_{16}V_{ds}^2+a_{17}V_{ds}^3\} \quad (4)$$

$$f_2(V_{g2s},V_{ds}) = \{(b_0+b_1V_{ds})+(b_2+b_3V_{ds})V_{g2s} + (b_4+b_5V_{ds})V_{g2s}^2+(b_6+b_7V_{ds})V_{g2s}^3 + (b_8+b_9V_{ds})V_{g2s}^4+(b_{10}+b_{11}V_{ds})V_{g2s}^5 + (b_{12}+b_{13}V_{ds})V_{g2s}^6\}\{b_{14}+b_{15}V_{ds}+b_{16}V_{ds}^2+b_{17}V_{ds}^3\} \quad (5)$$

$$f_3(V_{g1s},V_{g2s},V_{ds}) = \tanh(c_0V_{ds})+c_1(c_2+c_3V_{g1s} + c_4V_{g1s}^2+c_5V_{g1s}^3+c_6V_{g1s}^4)+c_7(c_8+c_9V_{g2s} + c_{10}V_{g2s}^2+c_{11}V_{g2s}^3+c_{12}V_{g2s}^4) \quad (6)$$

The a_i, b_i, and c_i coefficients are the model fitting parameters that can be simultaneously extracted by the least-squares method.

III. THE RF DRAIN CURRENT GENERATOR

To model the SGFET RF drain current, Winson [8] concluded that using one current source $I_d^{RF}(V_{gs},V_{ds})$ can not simultaneously model both $g_m^{RF}(V_{gs},V_{ds})$ and $g_d^{RF}(V_{gs},V_{ds})$ with good accuracy. To increase the accuracy of modeling the RF drain current of the SGFET, Winson [8] used two parallel current sources (connected between the source and the drain terminals) in the SGFET large-signal model. Each of these sources individually models g_m^{RF} and g_d^{RF}, and together will model the RF drain current.

In this work, the authors extend Winson's technique [8] to model the DGFET RF drain current, $I_d^{RF}(V_{gs1},V_{gs2},V_{ds})$. Three parallel current sources I_{gm1}, I_{gm2}, and I_{gds} are used to model $I_d^{RF}(V_{gs1},V_{gs2},V_{ds})$ of the DGFET. The current sources I_{gm1}, I_{gm2}, and I_{gds} are used to model the transconductance g_{m1}^{RF}, the transconductance g_{m2}^{RF}, and the output conductance g_{ds}^{RF} respectively.

The data for $g_{m1}^{RF}(V_{gs1},V_{gs2},V_{ds})$, $g_{m2}^{RF}(V_{gs1},V_{gs2},V_{ds})$, and $g_{ds}^{RF}(V_{gs1},V_{gs2},V_{ds})$ are extracted from the measured 3-port S-parameters using a new DGFET small-signal model introduced by the authors (to be submitted for publication):

$$[Y] = \begin{bmatrix} g_{11}+j\omega C_{11} & g_{12}+j\omega C_{12} & g_{13}+j\omega C_{13} \\ g_{21}+j\omega C_{21} & g_{22}+j\omega C_{22} & g_{23}+j\omega C_{23} \\ g_{m1}^{RF}+j\omega C_{31} & g_{m2}^{RF}+j\omega C_{32} & g_{ds}^{RF}+j\omega C_{33} \end{bmatrix} \quad (7)$$

where [Y] is the 3-port intrinsic admittance matrix of the DGFET.

Using I_{gm1}, I_{gm2}, and I_{gds} to independently model $I_d^{RF}(V_{gs1},V_{gs2},V_{ds})$ will encounter inconsistency problems between the small-signal and the large-signal models. The linearization of each of these current sources will generate other conductances and transconductances, which are, undesired components. For example, the linearization of I_{gm1} produces two transconductances g_{m1}^{RF} and $g_{m11} = \partial I_{gm1}/\partial V_{g2s}$, and a conductance $g_{m12} = \partial I_{gm1}/\partial V_{ds}$. The "transcapacitance-nulling technique" [9] is used to eliminate these undesired components.

The general equations used to model I_{gm1}, I_{gm2}, and I_{gds} are

$$I_{gm1}(V_{g1s},V_{g2s},V_{ds}) = A_1(V_{g1s},V_{g2s},V_{ds})-A_1(V_{g1s0},V_{g2s},V_{ds}) \quad (8)$$

$$I_{gm2}(V_{g1s},V_{g2s},V_{ds}) = A_2(V_{g1s},V_{g2s},V_{ds})-A_2(V_{g1s},V_{g2s0},V_{ds}) \quad (9)$$

$$I_{gds}(V_{g1s},V_{g2s},V_{ds}) = A_3(V_{g1s},V_{g2s},V_{ds})-A_3(V_{g1s},V_{g2s},V_{ds0}) \quad (10)$$

where $(V_{g1s0}, V_{g2s0}, V_{ds0})$ is the quiescent bias point.

From (8) it is easy to see that:

$$\frac{\partial I_{gm1}}{\partial V_{g1s}} = \frac{\partial A_1}{\partial V_{g1s}} = g_{m1}^{RF} \quad (11)$$

and

$$\left.\frac{\partial I_{gm1}}{\partial V_{g2s}}\right|_{V_{g1s}=V_{g1s0}} = \left.\frac{\partial I_{gm1}}{\partial V_{ds}}\right|_{V_{g1s}=V_{g1s0}} = 0 \quad (12)$$

In the same manner, it can be shown that when linearized, (9) and (10) will produce g_{m2}^{RF} and g_{ds}^{RF} respectively.

Equations (8), (9), and (10) represent general equations for the RF current sources I_{gm1}, I_{gm2}, and I_{gds}. To derive the specific equations for A_1, A_2, and A_3 a simple procedure is followed. Taking A_1 as an example, the following procedure is followed:

(i) Differentiate the DC drain current expression (3) with respect to V_{g1s} to determine g_{m1}^{DC}.

(ii) Use the g_{m1}^{DC} expression to fit the g_{m1}^{RF} data extracted from the measured S-parameters using the four-port small-signal model [9], and extract the model parameters a_i, b_i, and c_i that best fit g_{m1}^{RF}. Let the new parameters be a_{igm1}, b_{igm1}, and c_{igm1}.

(iii) The A_1 expression in this case will be the same expression (3) but with the a_{igm1}, b_{igm1}, and c_{igm1} parameters.

The same procedure is followed to derive A_2 and A_3.

IV. EXPERIMENTAL VERIFICATION

The developed model is used to fit the measured drain current of DGFETs of different topologies fabricated at Nortel Networks, Ottawa, Canada. Using a commercial fitting program, the fitting coefficients a_i, b_i, and c_i of (3) are determined.

Fig. 2 shows a comparison between the measured and the calculated DC drain current for a 6x100 μm DGFET. Very good agreement between the measured and the calculated data is shown. The expressions successfully model the RF drain current as well. This is clear from Fig. 3, where very good agreement between the modeled data and the extracted data of the RF transconductances and output conductance is shown. Very good agreement is also obtained at other bias points but space is not available here for their presentation.

V. CONCLUSION

An empirical model of the DGFET drain current is described. The frequency dispersion of the DGFET transconductances and output conductance is included in the new model. The model successfully simulates both the DC and the RF drain current of the DGFET. The model is tested on many devices with various gate widths and it showed very good agreement with the measured drain current over a wide range of bias conditions. This model is part of a new large-signal model of the DGFET.

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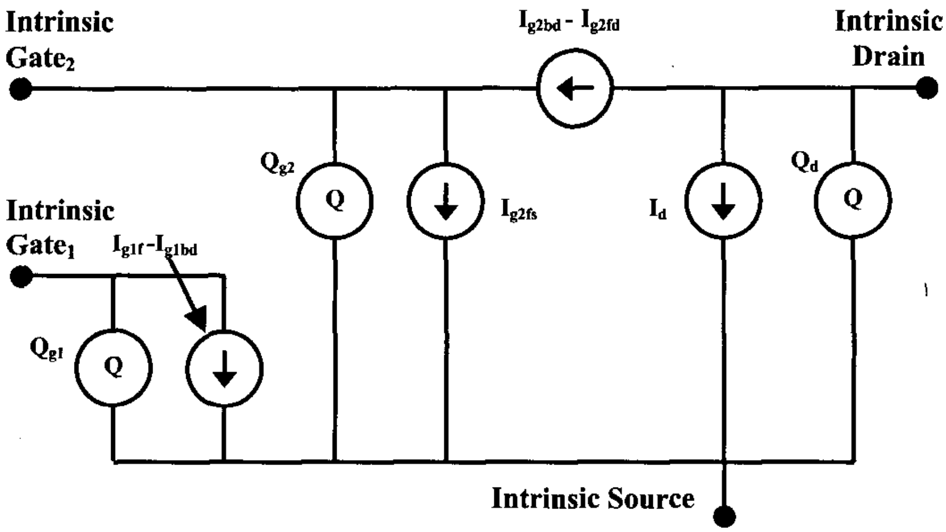

Fig. 1. Schematic of the dual-gate MESFET large-signal model.

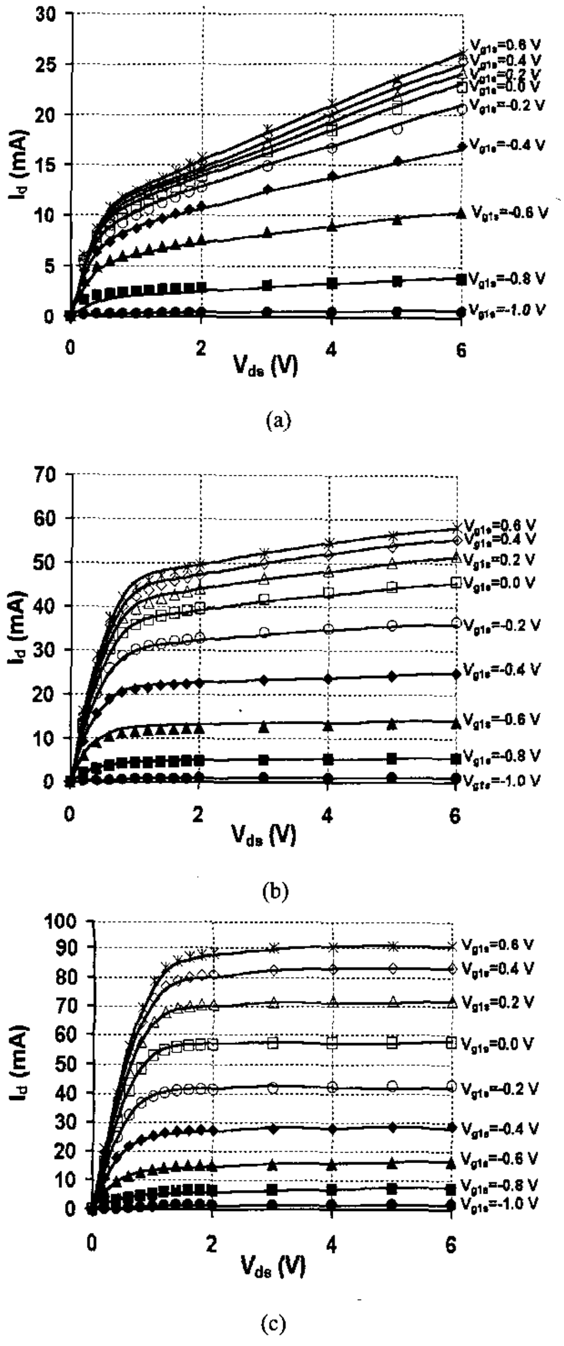

Fig. 2. Comparison of simulated (solid) and measured (symbols) DC-IV characteristics (at the extrinsic terminals) of a 6x100 μm DGFET as V_{ds} changes from 0 V to 6 V and V_{g1s} varies from −1.0 V to 0.6 V with steps of 0.2 V for V_{g2s} = -0.6 V (a), V_{g2s} = 0.0 V (b), and V_{g2s} = 0.6 V (c).

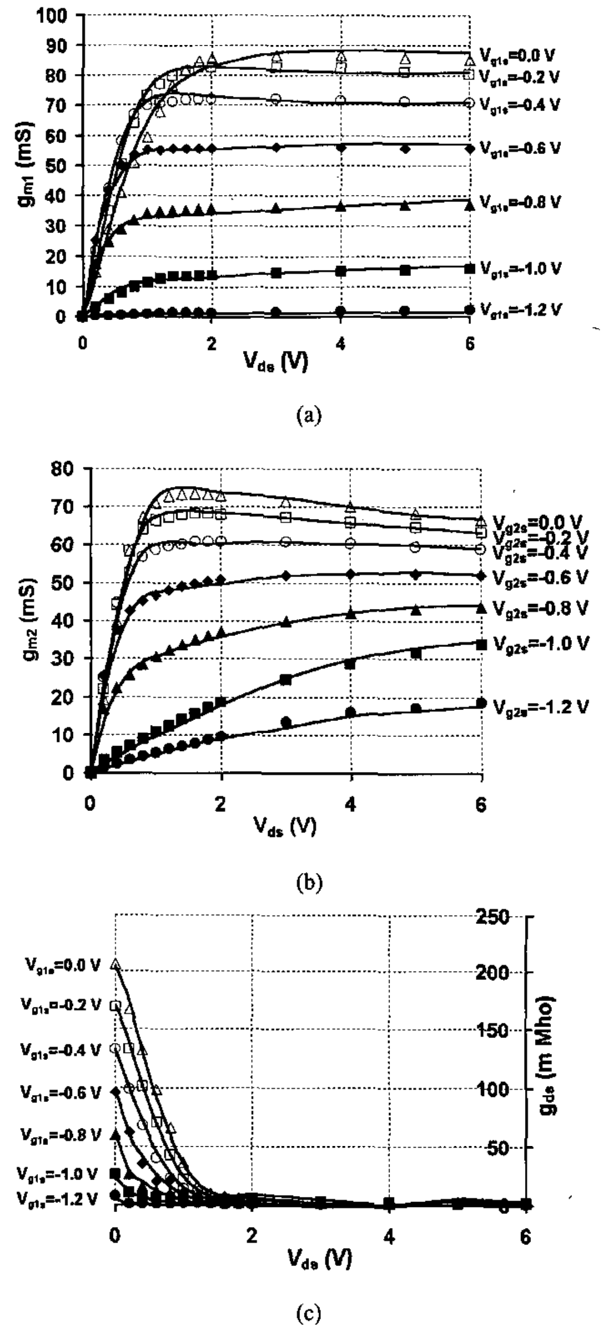

Fig. 3. Comparison of simulated (solid) and extracted (symbols) g_{m1}^{RF} (a), g_{ds}^{RF} (c) of a 6x100 μm DGFET at V_{g2s} = 0.6 V as V_{ds} changes from 0 V to 6 V and V_{g1s} varies from −1.2 V to 0 V with steps of 0.2 V, and g_{m2}^{RF} (b) of a 6x100 μm DGFET at V_{g1s} = 0.6 V as V_{ds} changes from 0 V to 6 V and V_{g2s} varies from −1.2 V to 0 V with steps of 0.2 V.